

Docket No: 14993.18

In re application of

) Art Unit

) 2816

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AJL:ds
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RICK D. NYDEGGER
BRENT P. LORIMER
THOMAS R. VUKSINICK
LARRY R. LAYCOCK
JONATHAN W. RICHARDS
DAVID R. WRIGHT
JOHN C. STRINGHAM
JOHN M. GUYNN
CHARLES L. ROBERTS
DANA L. TANGREN
ERIC L. MASCHOFF
CHARLES J. VEVERKA
ROBYN L. PHILLIPS
RICHARD C. GILMORE *
STERLING A. BRENNAN
R. BURNS ISRAELSEN
DAVID R. TODD
GREGORY M. TAYLOR
DAVID B. DELLENBACH
L. DAVID GRIFFIN
ADRIAN J. LEE
FRASER D. ROY
CARL T. REED

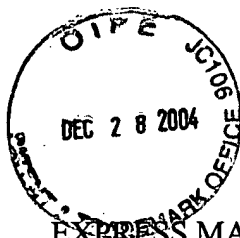


R. PARRISH FREEMAN, JR.
PETER F. MALEN, JR.
L. REX SEARS, PH.D.
WILLIAM R. RICHTER
ERIC M. KAMERATH
ROBERT E. AYCOCK
JENS C. JENKINS
KEVIN W. STINGER
WILLIAM J. ATHAY
MICHAEL B. DODD
RYAN D. BENSON
SARA D. JONES
TIGE KELLER
JANNA L. JENSEN
MATTHEW D. TODD
J. LAVAR OLDHAM
MICHAEL J. FRODSHAM
JOSEPH L. KRUPA
BRETT A. HANSEN
BRETT I. JOHNSON
MATTHEW A. BARLOW
WESLEY C. ROSANDER
ANDREW S. HANSEN
CHAD E. NYDEGGER
JOSEPH G. PIA
CLINTON E. DUKE
RYAN N. FARR *
JAMES B. BELSHE
ALISON B. MOHR
KIRK R. HARRIS
KEELY SCHNEITER
MICHAEL M. BALLARD
DAVID A. JONES
SHANE K. JENSEN
JONATHAN M. BENNS, PH.D.

VERNON R. RICE §
OF COUNSEL

WORKMAN | NYDEGGER

INTELLECTUAL PROPERTY ATTORNEYS



1000 EAGLE GATE TOWER
60 EAST SOUTH TEMPLE
SALT LAKE CITY, UTAH 84111
TELEPHONE: (801) 533-9800
FAX: (801) 328-1707
WEBSITE: HTTP://WWW.WNLAW.COM

EXPRESS MAIL LABEL NO.: EV 565664541 US PATENT APPLICATION
Docket No: 14993.18

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

Greg Scott et al.

Serial No.:

10/611,714

) Art Unit
) 2816

Filed:

July 1, 2003

Conf No.:

4464

For:

DOUBLE-SIDED EXTENDED DRAIN FIELD
EFFECT TRANSISTOR, AND INTEGRATED
OVERVOLTAGE AND REVERSE VOLTAGE
PROTECTION CIRCUIT THAT USES THE
SAME

Examiner:

Anh Quan Tra

TRANSMITTAL OF ISSUE FEE PAYMENT

Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Notice of Allowance and Issue Fee Due dated November 23, 2004, please find enclosed herewith the following items for filing in the United States Patent and Trademark Office in connection with the above identified patent application:

X Issue Fee Transmittal (PTOL-85B) submitted pursuant to 37 C.F.R. § 1.311.

☐ A Supplemental Declaration executed by the inventor(s) is submitted pursuant to 37 C.F.R. § 1.67.

☒ A Certificate of Deposit Under 37 C.F.R. § 1.8 is enclosed.

☐ Pursuant to the request for submission of formal drawings, enclosed are the following:

☐ A Letter to the Official Draftsperson;

☐ A set of _____ () sheets of formal drawings to replace the corresponding drawings originally filed with the subject application.

☐ A duplicate set of the _____ () sheets of formal drawings with the changes therein highlighted in red.

☒ PTO 2038 Credit Card form for \$1,715.00 is enclosed to cover:

☒ The \$1,370.00 government issue fee pursuant to 37 C.F.R. § 1.18.

☒ The \$300.00 government publication fee pursuant to 37 C.F.R. § 1.18.(d)

☒ The \$45.00 fee for fifteen (15) copies of the patent when issued.

☒ The Commission is hereby authorized to charge payment of any additional fees or credit any overpayment to Deposit Account No. 23-3178.

☒ A duplicate copy of this letter is enclosed.

Comments on Statement of Reasons for Allowance

On page 2 of the Examiner's Notice of Allowability, the Examiner has indicated that no prior art was found that "Claims 1-20 are allowable because the prior art fails to teach or suggest a circuit (such as figure 1) having a first and second double side extended drain FETs (102,102); and a first resistor R1 coupled

between the power supply and the body terminal of the first double side extended drain FET 102.”

Applicants respectfully submit that the claimed invention as set forth in each of the independent claims and the dependent claims must be read as a whole, and not as a single feature or subcombination of features which represent less than the entirety of the claimed invention as a whole. While a particular feature or subcombination of features referred to by the Examiner in the Statement of Reasons for Allowance may represent a basis for distinguishing the claimed invention over the prior art, Applicants further submit that this may not necessarily be the *sole* ground for distinguishing the claimed invention over the prior art of record. Accordingly, the Examiner’s statement should, in Applicants’ view, not be read as constituting or meaning that the invention can or should be reduced to a single “feature” of the invention or to a subcombination of features that is less than the entire invention claimed as a whole, nor that the single feature referenced by the Examiner or subcombination of features referenced by the Examiner in the Statement of Reasons for Allowance is the only or sole grounds for distinguishing the invention over the prior art of record.

Please address all future correspondence in connection with the above-identified patent application to the attention of the undersigned.

Dated this 28th day of December 2004.

Respectfully submitted,



Adrian J. Lee
Attorney for Applicant
Registration No. 42,785
Customer No. 022913